Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A method comprising:

initiating a direct memory access; and

successively transferring data from linked buffers in a first processor system to linked buffers in a second processor system.

Claim 2 (previously presented): The method of claim 1 wherein successively transferring data from linked buffers includes successively transferring data from buffers arranged in a linked list on the first processor system to buffers arranged in a linked list on the second processor system.

Claim 3 (original): The method of claim 2 including providing descriptors that indicate the status of each of said buffers.

Claim 4 (original): The method of claim 3 including providing flags that indicate whether a buffer is empty or full.

Claim 5 (previously presented): The method of claim 1 including transferring data between buffers within a cellular telephone.

Claim 6 (previously presented): The method of claim 5 including transferring data between the first processor system that includes a baseband processor and the second processor system that includes a multimedia processor of the cellular telephone.

Claim 7 (cancel)

Claim 8 (cancel)

Claim 9 (currently amended): The method of claim [[8]] 1 including generating an interrupt when a buffer is empty and data is to be transferred from the buffer, intercepting the interrupt, and automatically filling the buffer.

Claim 10 (original): The method of claim 9 including determining whether a buffer that is to receive data is full and if the buffer is full, automatically generating an interrupt, intercepting the interrupt, and automatically emptying the buffer.

Claim 11 (currently amended): An article comprising a medium ~~storing~~ to store instructions that enable a processor-based system to:

initiate a direct memory access; and

successively transfer data from linked buffers in a first processor system to linked buffers in a second processor system.

Claim 12 (previously presented): The article of claim 11 further storing instructions that enable the processor-based system to successively transfer data from linked buffers arranged in a linked list on the first processor system to buffers arranged in a linked list on the second processor system.

Claim 13 (original): The article of claim 12 further storing instructions that enable the processor-based system to provide descriptors that indicate the status of each of said buffers.

Claim 14 (original): The article of claim 13 further storing instructions that enable the processor-based system to provide flags that indicate whether a buffer is empty or full.

Claim 15 (previously presented): The article of claim 11 further storing instructions that enable the processor-based system to transfer data between buffers within a cellular telephone.

Claim 16 (previously presented): The article of claim 15 further storing instructions that enable the processor-based system to transfer data between the first processor system that includes a baseband processor and the second processor system that includes a multimedia processor of the cellular telephone.

Claim 17 (cancel)

Claim 18 (cancel)

Claim 19 (currently amended): The article of claim [[18]] 11 further storing instructions that enable the processor-based system to generate an interrupt when a buffer is

empty and data is to be transferred from the buffer, intercept the interrupt, and automatically fill the buffer.

Claim 20 (original): The article of claim 19 further storing instructions that enable the processor-based system to determine whether a buffer that is to receive data is full and if the buffer is full, automatically generate an interrupt, intercept the interrupt, and automatically empty the buffer.

Claim 21 (currently amended): A system comprising:

a processor; and

a storage coupled to said processor ~~storing~~ to store instructions that enable the processor to:

initiate a direct memory access; and

successively transfer data from linked buffers in a first processor system to linked buffers in a second processor system.

Claim 22 (previously presented): The system of claim 21 wherein said storage stores instructions that enable the processor to successively transfer data from linked buffers arranged in a linked list on the first processor system to buffers arranged in a linked list on the second processor system.

Claim 23 (original): The system of claim 22 wherein said storage stores instructions that enable the processor to provide descriptors that indicate the status of each of said buffers.

Claim 24 (original): The system of claim 23 wherein said storage stores instructions that enable the processor to provide flags that indicate whether a buffer is empty or full.

Claim 25 (previously presented): The system of claim 21 wherein said linked buffers are within a cellular telephone.

Claim 26 (original): The system of claim 25 wherein said processor is a baseband processor, said system further including a multimedia processor.

Claim 27 (cancel)

Claim 28 (cancel)

Claim 29 (currently amended): The system of claim [[28]] 21 wherein said storage stores instructions that enable the processor to generate an interrupt when a buffer is empty and data is to be transferred from the buffer, intercept the interrupt, and automatically fill the buffer.

Claim 30 (original): The system of claim 29 wherein said storage stores instructions that enable the processor to determine whether a buffer that is to receive data is full and if the buffer is full, automatically generate an interrupt, intercept the interrupt, and automatically empty the buffer.

Claim 31 (new): The method of claim 1, further comprising successively transferring the data via a first-in-first-out buffer in the first processor system to a first-in-first-out buffer in the second processor system.

Claim 32 (new): The method of claim 1, further comprising successively transferring the data via an internal bus of a wireless communication system comprising the first processor system and the second processor system.

Claim 33 (new): The article of claim 11, further storing instructions that enable the system to successively transfer the data via a first-in-first-out buffer in the first processor system to a first-in-first-out buffer in the second processor system.

Claim 34 (new): The article of claim 11, further storing instructions that enable the system to successively transfer the data via an internal bus of a wireless communication system comprising the first processor system and the second processor system.

Claim 35 (new): The system of claim 21 wherein the first processor system comprises a first-in-first-out buffer coupled to the linked buffers.

Claim 36 (new): The system of claim 21, wherein the system comprises a wireless communication system comprising the first processor system and the second processor system, the wireless communication system further comprising an internal bus to couple the first processor system and the second processor system.